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(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD

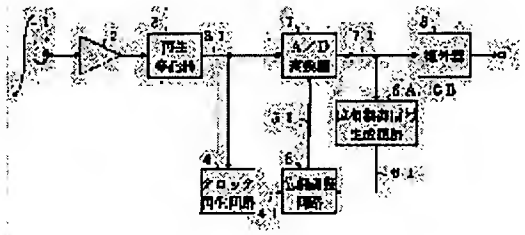
(72)Inventor : NAKATSU YOSHIHITO
OCHI ATSUO
NAKAGAKI HIROFUMI
USUKI NAOJI

(54) DATA DECODER

(57)Abstract:

PROBLEM TO BE SOLVED: To always provide stable data decoding by performing automatic control for always positioning a clock phase (detection timing) in the center of the opening part of an eye pattern.

SOLUTION: A reproducing signal from a recording medium 1 is equalized with PR (1, 0, -1) by a reproducing equalizer 3 and converted into a reproducing equalization signal. A clock reproducing circuit 4 outputs a reproducing clock synchronized with the timing of data identification to a phase adjustment circuit 5. A phase control signal generation circuit 6A detects a particular pattern from a reproducing digital signal outputted from an A/D converter 7 and then detects the advancing or delaying amount of a reproducing clock based on the amplitude or variance of a sampling value. Then, this phase shifting amount is provided as a phase control signal to the phase adjustment circuit 5. The phase adjustment circuit 5 provides a delay clock to the A/D converter 7 and performs control for A/D converting the reproducing signal by a correct timing.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The playback equalizing circuit which changes the regenerative signal from a record medium into a playback identification signal by the identification of a partial response property, The clock regenerative circuit which outputs the playback clock which synchronized with the timing of data discernment from the playback identification signal of said playback equalizing circuit, The phase adjustment circuit which performs a phase shift for the playback clock of said clock regenerative circuit according to a phase control signal, and outputs this as a delay clock, The A/D converter which samples said playback identification signal with the delay clock of said phase adjustment circuit, and is changed into a playback digital signal, The phase control signal generation circuit which outputs the phase control signal which detects a clock phase shift based on level change of the playback digital signal outputted from said A/D converter, and reduces said clock phase shift to said phase adjustment circuit, Data decode equipment characterized by providing the decoder which decodes the playback digital signal of said A/D converter to data.
[Claim 2] Said phase control signal generation circuit The inside of the playback digital signal of said A/D converter, The sign train from which signal level becomes symmetrical with order as a point by return [timing / specific] is extracted as a specific pattern sign. The phase shift detector which detects a clock phase shift based on level change of said specific pattern sign sampled with the delay clock of said phase adjustment circuit, Data decode equipment according to claim 1 characterized by having the control signal conversion circuit which outputs a phase control signal to said phase adjustment circuit so that the phase shift detected in said phase shift detector may be reduced.
[Claim 3] When said phase control signal generation circuit samples the digital regenerative signal of said A/D converter with the playback clock of said clock regenerative circuit, Whenever [dispersion / which computes whenever / over reference signal level / dispersion / from the sampling value, and judges the size of whenever / dispersion / in level] A size judging circuit, Signal level extracts the sign train which carries out partial change as a specific pattern sign to the shape of a sine wave among the playback digital signals of said A/D converter. The phase shift detector which detects a clock phase shift based on level change of said specific pattern sign sampled with the delay clock of said phase adjustment circuit, When whenever [dispersion] is judged whenever [said dispersion] in a size judging circuit with the sweep signal generating circuit which generates the scanning signal of the range whose amount of phase shifts is 0 degree - 360 degrees to be size, When the scanning signal of said sweep signal generating circuit is chosen and whenever [dispersion] is judged to be smallness, Data decode equipment according to claim 1 characterized by having the change-over circuit which chooses and outputs the clock phase shift signal of said phase shift detector, and the control signal conversion circuit which gives the output chosen to said phase adjustment circuit in said change-over circuit as a phase control signal.
[Claim 4] Said phase shift detector is the timing t0 of the playback clock of said clock regenerative circuit to the predetermined phase range. When making into a specific pattern sign the sign train from which signal level becomes symmetrical with order as a point by return, The pattern detector which

inputs the playback digital signal of said A/D converter, and detects said specific pattern sign, When setting to F (t0-) and F (t0+) signal level which sampled the specific pattern sign detected in said pattern detector with the delay clock of the phase adjustment circuit located before and after said timing t0, respectively, Data decode equipment according to claim 2 or 3 characterized by having the comparator which measures the symmetry of said F (t0-) and F (t0+), and the total circuit which the comparison result of said comparator is made to correspond in the direction of a phase shift of said playback clock, and totals.

[Claim 5] Said decoder is data decode equipment of claim 1-4 characterized by performing Viterbi decoding given in any 1 term.

[Claim 6] Said playback equalizing circuit is data decode equipment of claim 1 characterized by partial response properties being PR (1, 0, -1).

[Claim 7] The specific pattern sign which the digital regenerative signal of said A/D converter is a signal corresponding to 3 value signals of level (0 -1, 1), and said pattern detector detects Four continuous signal level is the sign trains corresponding to (0, 1 and 1, 0), and (0, -1, -1 and 0). Said comparator circuit Data decode equipment of claim 1-4 characterized by being what compares the 2nd and the 3rd signal level among four signal level given in any 1 term.

[Claim 8] The specific pattern sign which the digital regenerative signal of said A/D converter is a signal corresponding to 3 value signals of level (0 -1, 1), and said pattern detector detects It is data decode equipment of claims 1-4 which two continuous signal level is the sign trains corresponding to (1, 1), and (-1, -1), and are characterized by said comparator circuit being what compares two signal level given in any 1 term.

[Claim 9] A size judging circuit is data decode equipment of claim 3 characterized by what is judged with the ratio to which the level of the playback digital signal which said A/D converter outputs exists in the predetermined level range whenever [said dispersion].

[Claim 10] Said specific pattern sign is data decode equipment of claim 2-4 characterized by what is intermittently recorded on the record section of said record medium given in any 1 term.

[Claim 11] Said phase control signal generation circuit is data decode equipment according to claim 2 or 3 characterized by not changing level of said phase control signal in the predetermined period containing said discontinuity when discontinuity exists in the record section of said record medium.

[Claim 12] Said phase control signal generation circuit is data decode equipment according to claim 2 or 3 by which it is holding [usually]-at time of adjustable-speed playback of said record medium-level of phase control signal at time of playback characterized.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the data decode equipment which reproduces a signal from record media, such as a magnetic tape, and obtains image data and voice data.
[0002]
[Description of the Prior Art] There is a partial response method (PR) as a means to reproduce the signal recorded on the magnetic-recording medium, and to decode the same data stream as the time of record. It equalizes like and this identifies the data stream at the time of record from the signal corresponding to multiple-value level which has a predetermined intersymbol interference for a regenerative signal. Below, it is a kind of a partial response and the decode approach of the data using PR (1, 0, -1) with the frequency characteristics near a magnetic-recording system is explained.
[0003] Ushiro's data stream which passed through PURIKODA shown in drawing 9 is recorded on the magnetic-recording medium. for example, an input data train ... 001010 ... PURIKODA ... 001000 -- it is changed into ... and recorded. When D is the delay operation of a bit period, for the regenerative signal from a magnetic-recording medium, the frequency characteristics which let record playback pass are 1-D2. Playback identification is carried out so that it may become. this -- an isolated pulse ... 001000 -- the regenerative signal from the magnetic-recording medium by which ... was recorded ... 0010-10 -- it means equalizing in ...
[0004] As shown in the eye pattern of drawing 10 (a), the reference signal level in data discernment timing playback identification Ushiro's signal - It becomes a signal corresponding to 3 value signals of 1, 0, and +1. The level of a signal is a thing corresponding to **1 Data" 1" It is a thing corresponding to level 0 Data" 0" By identifying, it can decode to the original data stream. As mentioned above, although decode of the data using a partial response was explained briefly, it is described by reference (Eto, Mita, and Doi: "a digital video record technique", Nikkan Kogyo Shimbun, p36-38, p46-p48) in detail.
[0005] As shown in drawing 10 (a), the aperture width of the direction of a time-axis of the eye pattern in a partial response method is narrow compared with the integral detection method from the former shown in drawing 10 (b). For this reason, if the clock phase which shows detection timing shifts under the effect of the temperature characteristic of the clock playback section etc., an error rate will deteriorate sharply. Then, the magnetic recording medium indicated by JP,7-192404,A is one of those were controlled so that detection timing was stabilized and located focusing on opening of an eye pattern (henceforth an eye core). This detects and carries out feedback control of the phase shift of a clock from the specific pattern contained in a playback digital signal.
[0006]
[Problem(s) to be Solved by the Invention] However, the drawing-in time amount of the clock phase of a specific pattern is proportional to the occurrence frequency of the specific pattern contained in a playback digital signal. For this reason, with the above magnetic recording media, the occurrence frequency of a specific pattern is raised and compaction of the drawing-in time amount of a clock phase is aimed at by carrying out encoding processing of the record signal. In this case, the ratio of the

effective data contained in record data will fall.
[0007] Moreover, although the ratio of an effective data does not fall if encoding processing which raises the occurrence frequency of a specific pattern is not carried out, the drawing-in time amount of a clock phase will become large. For this reason, a reset time until it recovers to a good error rate in discontinuity of a regenerative signal, such as the drop out section resulting from the blemish on the head switching section in a digital video tape recorder or a record medium, will become large. Moreover, since it is also possible that a specific pattern is not generated over long duration, a clock phase will shift in the period and an error rate will deteriorate.
[0008] Drawing 4 is the explanatory view showing the relation between detection timing and whenever [dispersion / in a playback identification signal] in an eye pattern. As an initial clock phase shows at the time of day of the dotted line (a) of drawing 4 , when it shifts greatly from an eye core, though a clock phase may not be drawn focusing on an eye and draws, most time amount is required.
[0009] This invention aims at realizing data decode equipment without the need of being made in view of such a conventional trouble, carrying out regulating automatically so that the detection timing of a playback clock may always come focusing on an eye, it always being stabilized, and being able to obtain the low data of an error rate, and making record data into redundancy.
[0010]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem invention of this application according to claim 1 The playback equalizing circuit which changes the regenerative signal from a record medium into a playback identification signal by the identification of a partial response property, The clock regenerative circuit which outputs the playback clock which synchronized with the timing of data discernment from the playback identification signal of said playback equalizing circuit, The phase adjustment circuit which performs a phase shift for the playback clock of said clock regenerative circuit according to a phase control signal, and outputs this as a delay clock, The A/D converter which samples said playback identification signal with the delay clock of said phase adjustment circuit, and is changed into a playback digital signal, The phase control signal generation circuit which outputs the phase control signal which detects a clock phase shift based on level change of the playback digital signal outputted from said A/D converter, and reduces said clock phase shift to said phase adjustment circuit, It is characterized by providing the decoder which decodes the playback digital signal of said A/D converter to data.
[0011] In invention of this application according to claim 2, moreover, said phase control signal generation circuit The sign train from which signal level becomes symmetrical with order as a point by return [timing / specific] among the playback digital signals of said A/D converter is extracted as a specific pattern sign. The phase shift detector which detects a clock phase shift based on level change of said specific pattern sign sampled with the delay clock of said phase adjustment circuit, It is characterized by having the control signal conversion circuit which outputs a phase control signal to said phase adjustment circuit so that the phase shift detected in said phase shift detector may be reduced.
[0012] In invention of this application according to claim 3, moreover, said phase control signal generation circuit When the digital regenerative signal of said A/D converter is sampled with the playback clock of said clock regenerative circuit, Whenever [dispersion / which computes whenever / over reference signal level / dispersion / from the sampling value, and judges the size of whenever / dispersion / in level] A size judging circuit, Signal level extracts the sign train which carries out partial change as a specific pattern sign to the shape of a sine wave among the playback digital signals of said A/D converter. The phase shift detector which detects a clock phase shift based on level change of said specific pattern sign sampled with the delay clock of said phase adjustment circuit, When whenever [dispersion] is judged whenever [said dispersion] in a size judging circuit with the sweep signal generating circuit which generates the scanning signal of the range whose amount of phase shifts is 0 degree - 360 degrees to be size, When the scanning signal of said sweep signal generating circuit is chosen and whenever [dispersion] is judged to be smallness, It is characterized by having the change-over circuit which chooses and outputs the clock phase shift signal of said phase shift detector, and the control signal conversion circuit which gives the output chosen to said phase adjustment circuit in said

change-over circuit as a phase control signal.
[0013] In invention of this application according to claim 4, moreover, said phase shift detector Timing t0 of the playback clock of said clock regenerative circuit to the predetermined phase range When making into a specific pattern sign the sign train from which signal level becomes symmetrical with order as a point by return, The pattern detector which inputs the playback digital signal of said A/D converter, and detects said specific pattern sign, About the specific pattern sign detected in said pattern detector, it is said timing t0. When setting to F (t0-) and F (t0+) signal level sampled with the delay clock of the phase adjustment circuit in which it is located forward and backward, respectively, It is characterized by having the comparator which measures the symmetry of said F (t0-) and F (t0+), and the total circuit which the comparison result of said comparator is made to correspond in the direction of a phase shift of said playback clock, and totals.
[0014] Moreover, in invention of this application according to claim 5, said decoder is characterized by performing Viterbi decoding.
[0015] Moreover, in invention of this application according to claim 6, said playback equalizing circuit is characterized by partial response properties being PR (1, 0, -1).
[0016] In invention of this application according to claim 7, moreover, the digital regenerative signal of said A/D converter The specific pattern sign which is a signal corresponding to 3 value signals of level (0 -1, 1), and said pattern detector detects Four continuous signal level is the sign trains corresponding to (0, 1 and 1, 0), and (0, -1, -1 and 0), and said comparator circuit is characterized by comparing the 2nd and the 3rd signal level among four signal level.
[0017] Moreover, in invention of this application according to claim 8, the specific pattern sign which the digital regenerative signal of said A/D converter is a signal corresponding to 3 value signals of level (0 -1, 1), and said pattern detector detects is a sign train corresponding to (1, 1), and (-1, -1) in two continuous signal level, and said comparator circuit is characterized by comparing two signal level.
[0018] Moreover, in invention of this application according to claim 9, a size judging circuit is characterized by what is judged with the ratio to which the level of the playback digital signal which said A/D converter outputs exists in the predetermined level range whenever [said dispersion].
[0019] Moreover, in invention of this application according to claim 10, said specific pattern sign is characterized by what is intermittently recorded on the record section of said record medium.
[0020] Moreover, by invention of this application according to claim 11, said phase control signal generation circuit is characterized by not changing level of said phase control signal in the predetermined period containing said discontinuity, when discontinuity exists in the record section of said record medium.
[0021] Moreover, in invention of this application according to claim 12, it is holding-usually-level of phase control signal at time of playback characterized by said phase control signal generation circuit at the time of adjustable-speed playback of said record medium.
[0022] Above, according to the configuration [like], clock playback drawn in a high speed from a playback identification signal is performed, by carrying out the phase shift of the playback clock based on the phase shift detection result by the playback digital signal, regulating automatically is carried out so that detection timing may always come focusing on an eye, and it is always stabilized, and the error rate of good data can be acquired.
[0023] When the clock phase is not contained in opening of an eye pattern when dispersion over the multiple-value reference level of the digital regenerative signal by which A/D conversion was carried out is large according to especially the configuration of claim 3 that is, the sweep of the clock phase is carried out until it goes into opening. When a clock phase goes into opening of an eye pattern when dispersion is small that is, by controlling so that a clock phase shift is detected and a clock phase consists of a digital regenerative signal focusing on an eye, a clock phase is always located focusing on an eye, and the error rate of good data can be acquired.
[0024]
[Embodiment of the Invention]
(Gestalt 1 of operation) The data decode equipment in the gestalt of operation of the 1st of this invention

is explained using a drawing. Drawing 1 is the block diagram showing the whole data decode equipment configuration in the gestalt of this operation. The digital data is recorded on the magnetic tape 1. The regenerative signal reproduced from this magnetic tape 1 is inputted into the playback equalizer 3 through a head amplifier 2. The playback equalizer 3 is equalized that it seems that it becomes the property of PR (1, 0, -1) of a regenerative signal. The playback equalizer 3 can consist of transversal filters of 5 - 10 tap extent. The playback identification signal 31 outputted from the playback equalizer 3 is inputted into the clock regenerative circuit 4, and the playback clock 41 in which detection timing is shown is generated.

[0025] Drawing 2 (1) is the wave form chart of the playback identification signal 31, and drawing 2 (2) is the wave form chart showing the phase relation of the playback clock 41 and the delay clock 51. The clock regenerative circuit 4 of drawing 1 is constituted including a phase DOROKKU loop-formation (PLL) circuit. This PLL circuit controls a playback clock so that the phase with which the playback identification signal 31 crossed the threshold level (**0.5) shown by the dotted line (a) of drawing 2 (1) and (b), and the phase of the playback clock from an internal oscillator are in agreement. Since the playback identification signal 31 is a signal which crosses threshold level (**0.5) at intervals of an average of 1-2 bits, a clock is reproducible at a high speed. If the playback identification signal 31 is observed synchronizing with the playback clock 41, an eye pattern as shown in drawing 2 (1) will be obtained.

[0026] The playback clock 41 is inputted into the phase adjustment circuit 5 of drawing 1 , and the delay clock 51 delayed by the phase corresponding to the level of the phase control signal 61 from phase control signal generation circuit 6A is outputted from the phase adjustment circuit 5. In this way, the delay clock 51 is outputted with a phase which the timing of A/D conversion suits focusing on the eye shown in drawing 2 . In addition, the phase adjustment circuit 5 can consist of the delay lines with the controllable amount of delay.

[0027] On the other hand, the playback identification signal 31 outputted from the playback equalizer 3 is inputted also into A/D converter 7. And A/D conversion of this playback identification signal 31 is carried out to the timing of the delay clock 51. The playback digital signal 71 outputted from A/D converter 7 is inputted into the phase control signal generation circuit 6 and a decoder 8. Phase control signal generation circuit 6A is a circuit which outputs the phase control signal 61 which detects a clock phase shift based on level change of the playback digital signal outputted from A/D converter 7, and reduces a clock phase shift to the phase adjustment circuit 5. The phase control signal 61 for controlling the phase of the delay clock 51 so that the timing of A/D conversion specifically becomes focusing on the eye of drawing 2 is generated.

[0028] Next, the concrete configuration and its actuation of phase control signal generation circuit 6A are explained. Drawing 3 is the block diagram showing the configuration of phase control signal generation circuit 6A. The playback digital signal 71 is inputted into the phase shift detector 10 in this Fig. The phase shift detector 10 is constituted by pattern detector 10a, the delay machines 10b, 10c, and 10d, comparator 10e, and 10f of counter circuits. The phase shift detector 10 is a circuit which detects a clock phase shift based on level change of the specific pattern sign which signal level extracted the sign train which becomes symmetrical with order as a specific pattern sign, and sampled with the delay clock of the phase adjustment circuit 5 as a point by return [timing / specific] among the playback digital signals of A/D converter 7.

[0029] Pattern detector 10a is the timing t0 of the playback clock of the clock regenerative circuit 4 to the predetermined phase range. When making into a specific pattern sign the sign train from which signal level becomes symmetrical with order as a point by return, it is the circuit which inputs the playback digital signal of A/D converter 7, and detects a specific pattern sign. The delay machines 10b, 10c, and 10d consist of 1-bit delay elements, respectively. The playback digital signal delayed 1 bit through delay machine 10b and the playback digital signal delayed 2 bits through the delay machines 10c and 10d are given to comparator 10e.

[0030] About the specific pattern sign detected by pattern detector 12a, comparator 10e is timing t0. When setting to F (t0-) and F (t0+) signal level sampled with the delay clock of the phase adjustment

circuit 5 in which it is located forward and backward, respectively, it is the circuit which measures the symmetry of F (t0-) and F (t0+).
[0031] In the phase shift detector 10, if it is first detected in pattern detector 10a as a specific pattern (1 0, -1, -0) of three value signal patterns (1 0, +1, +0), the amount of phase shifts will be detected. Drawing 5 is the explanatory view showing the relation between detection timing and whenever [dispersion / in a playback identification signal] in an eye pattern. If considering the case of a pattern (1 0, +1, +0) a playback digital signal is detected to the timing of the dotted line (c) of drawing 4 , detection timing will become focusing on an eye and the amplitude value of the playback digital signal inputted into comparator 10e will become like the round mark of drawing 5 (1). Like the dotted line (b) of drawing 4 , when detection timing is early, the amplitude value of the playback digital signal inputted into comparator 10e becomes like the round mark of drawing 5 (b). Furthermore, like the dotted line (d) of drawing 4 , when detection timing is late, the amplitude value of the playback digital signal inputted into comparator 10e becomes like the round mark of drawing 5 (d).
[0032] When the detection timing shown in drawing 5 (2) is based on eyes, the 2 or 3rd signal level in a pattern becomes the same. To it, when detection timing is early, the direction of the 3rd signal level becomes large, and when detection timing is late, the direction of the 2nd signal level becomes large. Therefore, comparator 10e is comparing the 2nd outputted through 10d of delay machines, and the 3rd signal level outputted through delay machine 10b, and can detect progress or delay of detection timing.
[0033] Since a noise is included in the playback digital signal 71, the comparison result in every time varies. For this reason, 10f of counter circuits has the function of the total circuit which the comparison result of comparator 10e is made to correspond in the direction of a phase shift of a playback clock, and totals. The level comparison result specifically outputted from comparator 10e over a fixed period is accumulated, and at least majority processing of a comparison result detects progress or delay of a phase.
[0034] A phase shift is detected by the approach with the same said of the case of a pattern (1 0, -1, -0). Moreover, since three or more -1 does not continue among [+1] 3 value level, respectively in PR (1, 0, -1), a pattern (+1, +1) can be detected and a phase shift can also be detected by comparing two signal level (-1, -1). The detection result of a phase shift is inputted into the updown counter circuit 13 of drawing 3 , and changes one step of level of the phase control signal 61 in the direction which reduces a phase shift.
[0035] The digital control signal outputted from the updown counter circuit 13 is changed into the control signal of an analog by D/A converter 14. Thereby, the playback digital signal 71 of drawing 1 turns into a signal by which was always stabilized and A/D conversion was carried out to the timing based on eyes. The updown counter circuit 13 and D/A converter 14 have the function of the control signal conversion circuit which outputs a phase control signal to the phase adjustment circuit 5 here so that the phase shift detected in the phase shift detector 10 may be reduced.
[0036] This playback digital signal 71 is inputted into a decoder 8, Viterbi decoding is carried out, and decode data are outputted. Viterbi decoding decodes the Euclidean distance of a regenerative-signal point and each reference signal point to the bit string corresponding to the probable pass (a state transition is shown) as an index rather than identifies data for every bit. Details, such as a principle of Viterbi decoding and a configuration of the Viterbi decoder, are described by the reference (Eto, Mita, and Doi: "a digital video record technique", Nikkan Kogyo Shimbun, p72-84) mentioned above.
[0037] Thus, the error rate of the good signal always stabilized by high-speed clock drawing in by signal discontinuity and the clock phase adjustment based on [stable] eyes can be secured by performing separately high-speed clock playback and clock phase adjustment based on the playback digital signal level as which a low speed is sufficient, without making record data into redundancy.
[0038] (Gestalt 2 of operation) Next, the data decode equipment in the gestalt of operation of the 2nd of this invention is explained using a drawing. The whole data decode equipment configuration in the gestalt of this operation is the same as that of drawing 1 . The difference from the gestalt of the 1st operation is only a phase control signal generation circuit. Drawing 6 is the block diagram of phase control signal generation circuit 6B in the gestalt of this operation. Phase control signal generation

circuit 6B is constituted by the size judging circuit 15, the phase shift detector 16, the sweep signal generating circuit 17, a change-over switch 18, the updown counter circuit 19, and D/A converter 20 whenever [dispersion].

[0039] Whenever [dispersion], the size judging circuit 15 is a circuit which computes whenever [over reference signal level / dispersion] from the sampling value, and judges the size of whenever [dispersion / in level], when the digital regenerative signal of A/D converter 7 is sampled with the playback clock of the clock regenerative circuit 4. That is, the playback digital signal 71 of 3 value reference level is inputted, an input signal is sampled with the delay clock 51 of drawing 1 , multiple-times detection of the level of a sampling point is carried out, and the size of dispersion is judged with the ratio to which the level exists in the predetermined level range. The phase shift detector 16 is the same circuit as the phase shift detector 10 shown in drawing 3 . The sweep signal generating circuit 17 is a circuit which generates the scanning signal of the range whose amount of phase shifts is 0 degree - 360 degrees.

[0040] A change-over switch 18 is a change-over circuit which chooses the scanning signal of the sweep signal generating circuit 17 when dispersion is judged whenever [dispersion] in the size judging circuit 15 to be size, and chooses the phase shift signal of the phase shift detector 16 when dispersion is judged to be smallness. It is the same as that of what indicates the output of the updown counter circuit 19 which inputs the output of a change-over switch 18, and the updown counter circuit 19 to be D/A converter 20 changed into an analog signal to drawing 3 .

[0041] Actuation of phase control signal generating circuit 6B of such a configuration is explained. The playback digital signal 71 is inputted into the size judging circuit 15 whenever [dispersion], and it measures how much the playback digital signal 71 varies to 3 value reference level (+1, 0, -1). And whenever [dispersion] judges whether it is larger than a predetermined value or small, and outputs a judgment result.

[0042] Since whenever [dispersion / in the signal level of a sampling point] is large when the detection timing of the delay clock 51 is out of eye opening like the dotted line (a) of drawing 4 , "it is :size whenever [dispersion]" is outputted. Since whenever [dispersion] is small when it is in eye opening to it, as shown in the dotted line (b) of drawing 4 , (c), and (d), "it is :smallness whenever [dispersion]" is outputted. "dispersion degree: In smallness", a change-over switch 18 is switched by the phase shift detector 16. When the phase was progressing and the phase shift detector 16 detects, phase control signal generating circuit 6B changes and outputs the level of the phase control signal 61 so that a phase may be delayed through the updown counter circuit 19 and D/A converter 20. Moreover, when the phase was behind in the phase shift detector 16 and it detects, phase control signal generating circuit 6B changes and outputs the level of the phase control signal 61 so that a phase may be advanced through the updown counter circuit 19 and D/A converter 20.

[0043] "dispersion degree: In size", a change-over switch 18 is switched by the sweep signal generating circuit 17. In the phase shift detector 16 described previously, since a phase shift is undetectable, the phase control signal 61 which carries out the sweep of all the range of phase control as shown in drawing 7 is outputted until detection timing enters into eye opening. If detection timing enters into eye opening in the middle of a phase sweep, it will be judged with "It is :smallness whenever [dispersion]." And after the delay clock 51 goes into eye opening, the level of the phase control signal 61 is controlled by actuation of the phase shift detector 16. Whatever the initial phase of the delay clock 51 is by this, regulating automatically is always carried out to the timing based on eyes.

[0044] Thus, when whenever [dispersion / in the playback digital signal 71 seen from the delay clock 51] is large, a clock phase is shifted to eye pattern opening by carrying out the sweep of the clock phase. And by tuning a phase finely focusing on an eye based on the level of a playback digital signal, a clock phase can be quickly drawn from any initial phases focusing on an eye. If it carries out like this, it is always stabilized and the low signal of an error rate can be acquired.

[0045] When a record data stream is random, three value signal patterns (1 0, +1, +0) or (1 0, -1, -0) the probability to generate is 1/32, and three value signal patterns (+1, +1) or (-1, -1) the probability to generate is 1/8. The response time for drawing a clock phase focusing on opening of an eye pattern is

determined by the occurrence frequency of the signal of this pattern. Therefore, in order to bring the response time forward, a part for the repeated data division including many signals of the specific pattern mentioned above is inserted intermittently. And it is good to record the data stream containing a part for these data division on a record medium. for example, it is shown in drawing 8 -- as -- as a playback identification signal -- 0, +1, and + -- what is necessary is just to insert repeat data-division P used as 1, 0, -1, -1, and ... in the specific part in 1 truck

[0046] Moreover, a record medium is a magnetic tape and stops actuation of the phase shift detectors 10 and 16 in a fixed period containing the part from which a regenerative signal becomes discontinuous like at the time of head switching at the time of playback of a magnetic tape. And if the level of the phase control signal 61 is held to this and coincidence, the bad influence in the discontinuity of a record section is avoidable. What is necessary is just to usually hold the level of the phase control signal 61 at the time of playback by the same reason at the time of adjustable-speed playback.

[0047] Although the gestalt of the 1st and the 2nd operation explained the case where a magnetic tape was used as a record medium, the same thing can say also in the magnetic disks and optical disks other than a magnetic tape.

[0048]

[Effect of the Invention] According to invention according to claim 1 to 12, high-speed clock drawing in by signal discontinuity and drawing in at the stable eye core can be performed as mentioned above by performing separately high-speed clock playback and clock phase adjustment based on the playback digital signal level as which a low speed is sufficient, without making record data into redundancy. By such clock phase adjustment, the low data of the always stabilized error rate are obtained.

[0049] Especially according to invention according to claim 3, by carrying out the sweep of the clock phase, when whenever [dispersion / in a playback digital signal] is large, after shifting a clock phase to eye pattern opening, based on the level of a playback digital signal, phase adjustment is carried out focusing on an eye. If it carries out like this, a clock phase can be quickly drawn focusing on an eye, and the low data of the always stabilized error rate will be obtained from any initial phases.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the data decode equipment which reproduces a signal from record media, such as a magnetic tape, and obtains image data and voice data.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] There is a partial response method (PR) as a means to reproduce the signal recorded on the magnetic-recording medium, and to decode the same data stream as the time of record. It equalizes like and this identifies the data stream at the time of record from the signal corresponding to multiple-value level which has a predetermined intersymbol interference for a regenerative signal. Below, it is a kind of a partial response and the decode approach of the data using PR (1, 0, -1) with the frequency characteristics near a magnetic-recording system is explained.
[0003] The data stream after passing through PURIKODA shown in drawing 9 is recorded on the magnetic-recording medium. for example, an input data train ... 001010 ... PURIKODA ... 001000 -- it is changed into ... and recorded. When D is the delay operation of a bit period, for the regenerative signal from a magnetic-recording medium, the frequency characteristics which let record playback pass are 1-D2. Playback identification is carried out so that it may become. this -- an isolated pulse ... 001000 -- the regenerative signal from the magnetic-recording medium by which ... was recorded ... 0010-10 -- it means equalizing in ...
[0004] As shown in the eye pattern of drawing 10 (a), the reference signal level in data discernment timing the signal after playback identification - It becomes a signal corresponding to 3 value signals of 1, 0, and +1. The level of a signal is a thing corresponding to **1 Data" 1" It is a thing corresponding to level 0 Data" 0" By identifying, it can decode to the original data stream. As mentioned above, although decode of the data using a partial response was explained briefly, it is reference (Eto, Mita, Doi :) in detail.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] According to invention according to claim 1 to 12, high-speed clock drawing in by signal discontinuity and drawing in at the stable eye core can be performed as mentioned above by performing separately high-speed clock playback and clock phase adjustment based on the playback digital signal level as which a low speed is sufficient, without making record data into redundancy. By such clock phase adjustment, the low data of the always stabilized error rate are obtained.
[0049] Especially according to invention according to claim 3, by carrying out the sweep of the clock phase, when whenever [dispersion / in a playback digital signal] is large, after shifting a clock phase to eye pattern opening, based on the level of a playback digital signal, phase adjustment is carried out focusing on an eye. If it carries out like this, a clock phase can be quickly drawn focusing on an eye, and the low data of the always stabilized error rate will be obtained from any initial phases.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the drawing-in time amount of the clock phase of a specific pattern is proportional to the occurrence frequency of the specific pattern contained in a playback digital signal. For this reason, with the above magnetic recording media, the occurrence frequency of a specific pattern is raised and compaction of the drawing-in time amount of a clock phase is aimed at by carrying out encoding processing of the record signal. In this case, the ratio of the effective data contained in record data will fall.
[0007] Moreover, although the ratio of an effective data does not fall if encoding processing which raises the occurrence frequency of a specific pattern is not carried out, the drawing-in time amount of a clock phase will become large. For this reason, a reset time until it recovers to a good error rate in discontinuity of a regenerative signal, such as the drop out section resulting from the blemish on the head switching section in a digital video tape recorder or a record medium, will become large. Moreover, since it is also possible that a specific pattern is not generated over long duration, a clock phase will shift in the period and an error rate will deteriorate.
[0008] Drawing 4 is the explanatory view showing the relation between detection timing and whenever [dispersion / in a playback identification signal] in an eye pattern. As an initial clock phase shows at the time of day of the dotted line (a) of drawing 4 , when it shifts greatly from an eye core, though a clock phase may not be drawn focusing on an eye and draws, most time amount is required.
[0009] This invention aims at realizing data decode equipment without the need of being made in view of such a conventional trouble, carrying out regulating automatically so that the detection timing of a playback clock may always come focusing on an eye, it always being stabilized, and being able to obtain the low data of an error rate, and making record data into redundancy.

[Translation done.]

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MEANS

[Means for Solving the Problem] In order to solve the above-mentioned technical problem invention of this application according to claim 1 The playback equalizing circuit which changes the regenerative signal from a record medium into a playback identification signal by the identification of a partial response property, The clock regenerative circuit which outputs the playback clock which synchronized with the timing of data discernment from the playback identification signal of said playback equalizing circuit, The phase adjustment circuit which performs a phase shift for the playback clock of said clock regenerative circuit according to a phase control signal, and outputs this as a delay clock, The A/D converter which samples said playback identification signal with the delay clock of said phase adjustment circuit, and is changed into a playback digital signal, The phase control signal generation circuit which outputs the phase control signal which detects a clock phase shift based on level change of the playback digital signal outputted from said A/D converter, and reduces said clock phase shift to said phase adjustment circuit, It is characterized by providing the decoder which decodes the playback digital signal of said A/D converter to data.
[0011] In invention of this application according to claim 2, moreover, said phase control signal generation circuit The sign train from which signal level becomes symmetrical with order as a point by return [timing / specific] among the playback digital signals of said A/D converter is extracted as a specific pattern sign. The phase shift detector which detects a clock phase shift based on level change of said specific pattern sign sampled with the delay clock of said phase adjustment circuit, It is characterized by having the control signal conversion circuit which outputs a phase control signal to said phase adjustment circuit so that the phase shift detected in said phase shift detector may be reduced.
[0012] In invention of this application according to claim 3, moreover, said phase control signal generation circuit When the digital regenerative signal of said A/D converter is sampled with the playback clock of said clock regenerative circuit, Whenever [dispersion / which computes whenever / over reference signal level / dispersion / from the sampling value, and judges the size of whenever / dispersion / in level] A size judging circuit, Signal level extracts the sign train which carries out partial change as a specific pattern sign to the shape of a sine wave among the playback digital signals of said A/D converter. The phase shift detector which detects a clock phase shift based on level change of said specific pattern sign sampled with the delay clock of said phase adjustment circuit, When whenever [dispersion] is judged whenever [said dispersion] in a size judging circuit with the sweep signal generating circuit which generates the scanning signal of the range whose amount of phase shifts is 0 degree - 360 degrees to be size, When the scanning signal of said sweep signal generating circuit is chosen and whenever [dispersion] is judged to be smallness, It is characterized by having the change-over circuit which chooses and outputs the clock phase shift signal of said phase shift detector, and the control signal conversion circuit which gives the output chosen to said phase adjustment circuit in said change-over circuit as a phase control signal.
[0013] In invention of this application according to claim 4, moreover, said phase shift detector Timing t0 of the playback clock of said clock regenerative circuit to the predetermined phase range When making into a specific pattern sign the sign train from which signal level becomes symmetrical with

order as a point by return, The pattern detector which inputs the playback digital signal of said A/D converter, and detects said specific pattern sign, About the specific pattern sign detected in said pattern detector, it is said timing t0. When setting to F (t0-) and F (t0+) signal level sampled with the delay clock of the phase adjustment circuit in which it is located forward and backward, respectively, It is characterized by having the comparator which measures the symmetry of said F (t0-) and F (t0+), and the total circuit which the comparison result of said comparator is made to correspond in the direction of a phase shift of said playback clock, and totals.
[0014] Moreover, in invention of this application according to claim 5, said decoder is characterized by performing Viterbi decoding.
[0015] Moreover, in invention of this application according to claim 6, said playback equalizing circuit is characterized by partial response properties being PR (1, 0, -1).
[0016] In invention of this application according to claim 7, moreover, the digital regenerative signal of said A/D converter The specific pattern sign which is a signal corresponding to 3 value signals of level (0 -1, 1), and said pattern detector detects Four continuous signal level is the sign trains corresponding to (0, 1 and 1, 0), and (0, -1, -1 and 0), and said comparator circuit is characterized by comparing the 2nd and the 3rd signal level among four signal level.
[0017] Moreover, in invention of this application according to claim 8, the specific pattern sign which the digital regenerative signal of said A/D converter is a signal corresponding to 3 value signals of level (0 -1, 1), and said pattern detector detects is a sign train corresponding to (1, 1), and (-1, -1) in two continuous signal level, and said comparator circuit is characterized by comparing two signal level.
[0018] Moreover, in invention of this application according to claim 9, a size judging circuit is characterized by what is judged with the ratio to which the level of the playback digital signal which said A/D converter outputs exists in the predetermined level range whenever [said dispersion].
[0019] Moreover, in invention of this application according to claim 10, said specific pattern sign is characterized by what is intermittently recorded on the record section of said record medium.
[0020] Moreover, by invention of this application according to claim 11, said phase control signal generation circuit is characterized by not changing level of said phase control signal in the predetermined period containing said discontinuity, when discontinuity exists in the record section of said record medium.
[0021] Moreover, in invention of this application according to claim 12, it is holding-usually-level of phase control signal at time of playback characterized by said phase control signal generation circuit at the time of adjustable-speed playback of said record medium.
[0022] Above, according to the configuration [like], clock playback drawn in a high speed from a playback identification signal is performed, by carrying out the phase shift of the playback clock based on the phase shift detection result by the playback digital signal, regulating automatically is carried out so that detection timing may always come focusing on an eye, and it is always stabilized, and the error rate of good data can be acquired.
[0023] When the clock phase is not contained in opening of an eye pattern when dispersion over the multiple-value reference level of the digital regenerative signal by which A/D conversion was carried out is large according to especially the configuration of claim 3 that is, the sweep of the clock phase is carried out until it goes into opening. When a clock phase goes into opening of an eye pattern when dispersion is small that is, by controlling so that a clock phase shift is detected and a clock phase consists of a digital regenerative signal focusing on an eye, a clock phase is always located focusing on an eye, and the error rate of good data can be acquired.
[0024]
[Embodiment of the Invention]
(Gestalt 1 of operation) The data decode equipment in the gestalt of operation of the 1st of this invention is explained using a drawing. Drawing 1 is the block diagram showing the whole data decode equipment configuration in the gestalt of this operation. The digital data is recorded on the magnetic tape 1. The regenerative signal reproduced from this magnetic tape 1 is inputted into the playback equalizer 3 through a head amplifier 2. The playback equalizer 3 is equalized that it seems that it becomes the

property of PR (1, 0, -1) of a regenerative signal. The playback equalizer 3 can consist of transversal filters of 5 - 10 tap extent. The playback identification signal 31 outputted from the playback equalizer 3 is inputted into the clock regenerative circuit 4, and the playback clock 41 in which detection timing is shown is generated.

[0025] Drawing 2 (1) is the wave form chart of the playback identification signal 31, and drawing 2 (2) is the wave form chart showing the phase relation of the playback clock 41 and the delay clock 51. The clock regenerative circuit 4 of drawing 1 is constituted including a phase DOROKKU loop-formation (PLL) circuit. This PLL circuit controls a playback clock so that the phase with which the playback identification signal 31 crossed the threshold level (**0.5) shown by the dotted line (a) of drawing 2 (1) and (b), and the phase of the playback clock from an internal oscillator are in agreement. Since the playback identification signal 31 is a signal which crosses threshold level (**0.5) at intervals of an average of 1-2 bits, a clock is reproducible at a high speed. If the playback identification signal 31 is observed synchronizing with the playback clock 41, an eye pattern as shown in drawing 2 (1) will be obtained.

[0026] The playback clock 41 is inputted into the phase adjustment circuit 5 of drawing 1 , and the delay clock 51 delayed by the phase corresponding to the level of the phase control signal 61 from phase control signal generation circuit 6A is outputted from the phase adjustment circuit 5. In this way, the delay clock 51 is outputted with a phase which the timing of A/D conversion suits focusing on the eye shown in drawing 2 . In addition, the phase adjustment circuit 5 can consist of the delay lines with the controllable amount of delay.

[0027] On the other hand, the playback identification signal 31 outputted from the playback equalizer 3 is inputted also into A/D converter 7. And A/D conversion of this playback identification signal 31 is carried out to the timing of the delay clock 51. The playback digital signal 71 outputted from A/D converter 7 is inputted into the phase control signal generation circuit 6 and a decoder 8. Phase control signal generation circuit 6A is a circuit which outputs the phase control signal 61 which detects a clock phase shift based on level change of the playback digital signal outputted from A/D converter 7, and reduces a clock phase shift to the phase adjustment circuit 5. The phase control signal 61 for controlling the phase of the delay clock 51 so that the timing of A/D conversion specifically becomes focusing on the eye of drawing 2 is generated.

[0028] Next, the concrete configuration and its actuation of phase control signal generation circuit 6A are explained. Drawing 3 is the block diagram showing the configuration of phase control signal generation circuit 6A. The playback digital signal 71 is inputted into the phase shift detector 10 in this Fig. The phase shift detector 10 is constituted by pattern detector 10a, the delay machines 10b, 10c, and 10d, comparator 10e, and 10f of counter circuits. The phase shift detector 10 is a circuit which detects a clock phase shift based on level change of the specific pattern sign which signal level extracted the sign train which becomes symmetrical with order as a specific pattern sign, and sampled with the delay clock of the phase adjustment circuit 5 as a point by return [timing / specific] among the playback digital signals of A/D converter 7.

[0029] Pattern detector 10a is the timing t0 of the playback clock of the clock regenerative circuit 4 to the predetermined phase range. When making into a specific pattern sign the sign train from which signal level becomes symmetrical with order as a point by return, it is the circuit which inputs the playback digital signal of A/D converter 7, and detects a specific pattern sign. The delay machines 10b, 10c, and 10d consist of 1-bit delay elements, respectively. The playback digital signal delayed 1 bit through delay machine 10b and the playback digital signal delayed 2 bits through the delay machines 10c and 10d are given to comparator 10e.

[0030] About the specific pattern sign detected by pattern detector 12a, comparator 10e is timing t0. When setting to F (t0-) and F (t0+) signal level sampled with the delay clock of the phase adjustment circuit 5 in which it is located forward and backward, respectively, it is the circuit which measures the symmetry of F (t0-) and F (t0+).

[0031] In the phase shift detector 10, if it is first detected in pattern detector 10a as a specific pattern (1 0, -1, -0) of three value signal patterns (1 0, +1, +0), the amount of phase shifts will be detected.

Drawing 5 is the explanatory view showing the relation between detection timing and whenever [dispersion / in a playback identification signal] in an eye pattern. If considering the case of a pattern (1 0, +1, +0) a playback digital signal is detected to the timing of the dotted line (c) of drawing 4 , detection timing will become focusing on an eye and the amplitude value of the playback digital signal inputted into comparator 10e will become like the round mark of drawing 5 (1). Like the dotted line (b) of drawing 4 , when detection timing is early, the amplitude value of the playback digital signal inputted into comparator 10e becomes like the round mark of drawing 5 (b). Furthermore, like the dotted line (d) of drawing 4 , when detection timing is late, the amplitude value of the playback digital signal inputted into comparator 10e becomes like the round mark of drawing 5 (d).

[0032] When the detection timing shown in drawing 5 (2) is based on eyes, the 2 or 3rd signal level in a pattern becomes the same. To it, when detection timing is early, the direction of the 3rd signal level becomes large, and when detection timing is late, the direction of the 2nd signal level becomes large. Therefore, comparator 10e is comparing the 2nd outputted through 10d of delay machines, and the 3rd signal level outputted through delay machine 10b, and can detect progress or delay of detection timing.

[0033] Since a noise is included in the playback digital signal 71, the comparison result in every time varies. For this reason, 10f of counter circuits has the function of the total circuit which the comparison result of comparator 10e is made to correspond in the direction of a phase shift of a playback clock, and totals. The level comparison result specifically outputted from comparator 10e over a fixed period is accumulated, and at least majority processing of a comparison result detects progress or delay of a phase.

[0034] A phase shift is detected by the approach with the same said of the case of a pattern (1 0, -1, -0). Moreover, since three or more -1 does not continue among [+1] 3 value level, respectively in PR (1, 0, -1), a pattern (+1, +1) can be detected and a phase shift can also be detected by comparing two signal level (-1, -1). The detection result of a phase shift is inputted into the updown counter circuit 13 of drawing 3 , and changes one step of level of the phase control signal 61 in the direction which reduces a phase shift.

[0035] The digital control signal outputted from the updown counter circuit 13 is changed into the control signal of an analog by D/A converter 14. Thereby, the playback digital signal 71 of drawing 1 turns into a signal by which was always stabilized and A/D conversion was carried out to the timing based on eyes. The updown counter circuit 13 and D/A converter 14 have the function of the control signal conversion circuit which outputs a phase control signal to the phase adjustment circuit 5 here so that the phase shift detected in the phase shift detector 10 may be reduced.

[0036] This playback digital signal 71 is inputted into a decoder 8, Viterbi decoding is carried out, and decode data are outputted. Viterbi decoding decodes the Euclidean distance of a regenerative-signal point and each reference signal point to the bit string corresponding to the probable pass (a state transition is shown) as an index rather than identifies data for every bit. It is the reference (Eto, Mita, Doi :) mentioned above about details, such as a principle of Viterbi decoding, and a configuration of the Viterbi decoder.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the configuration of the data decode equipment in the gestalt of the 1st and operation of the 2nd of this invention.
[Drawing 2] It is an eye pattern in a partial response PR (1, 0, -1).
[Drawing 3] It is the block diagram showing the configuration of the phase control signal generation circuit in the gestalt of the 1st operation.
[Drawing 4] In an eye pattern, it is the explanatory view showing the relation between detection timing and whenever [dispersion / in a playback identification signal].
[Drawing 5] In the phase control signal generation circuit of the gestalt of the 1st operation, it is the explanatory view showing the relation of a gap between a playback digital signal and detection timing.
[Drawing 6] It is the block diagram showing the configuration of the phase control signal generation circuit in the gestalt of the 2nd operation.
[Drawing 7] It is the wave form chart of the scanning signal used for the phase control signal generation circuit of the gestalt of the 2nd operation.
[Drawing 8] It is the schematic diagram of the repeat data division which inserted the specific pattern.
[Drawing 9] It is the block diagram of PURIKODA which performs PURIKODO processing before record in PR (1, 0, -1). .
[Drawing 10] It is an explanatory view for explaining the difference between the eye pattern of 3 value signals in PR (1, 0, -1) identification, and the eye pattern of the binary signal in integral identification.
[Description of Notations]
1 Magnetic Tape
2 Head Amplifier
3 Playback Equalizer
4 Clock Regenerative Circuit
5 Phase Adjustment Circuit
6A, 6B Phase control signal generation circuit
7 A/D Converter
8 Decoder
10 16 Phase shift detector
10a Pattern detector
10b-10d Delay machine
10e Comparator
10f Counter circuit
13 19 Updown counter circuit
14 20 D/A converter
15 It is Size Judging Circuit whenever [Dispersion].
17 Sweep Signal Generating Circuit
18 Change-over Switch

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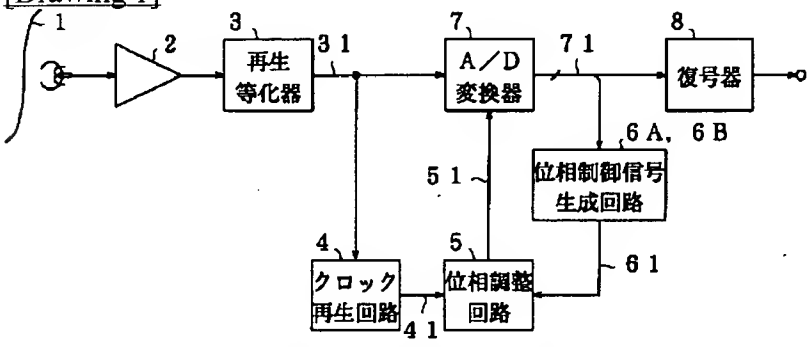
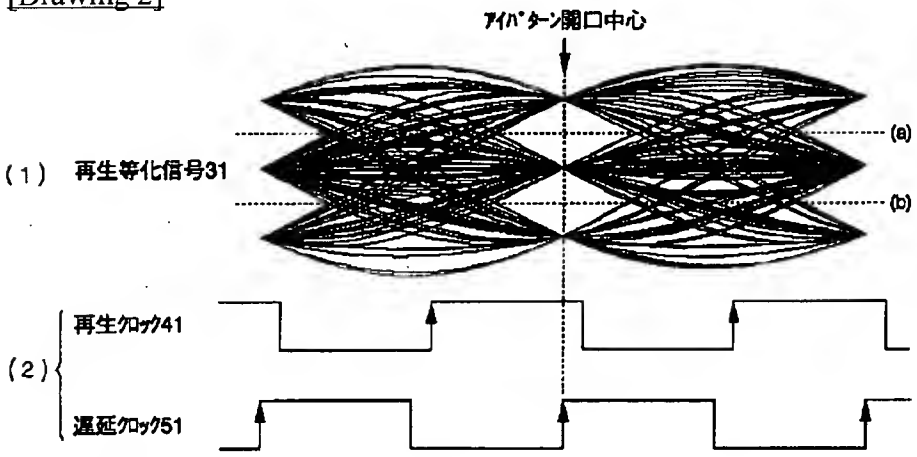
DRAWINGS

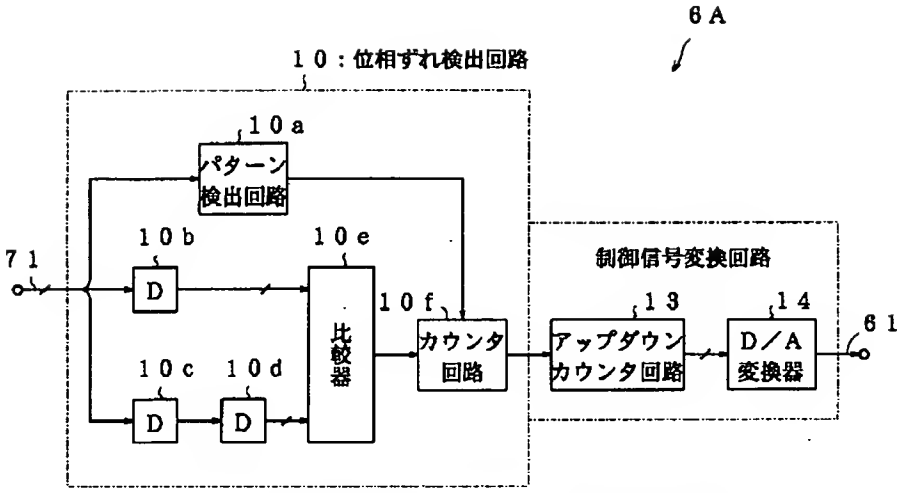
[Drawing 1]



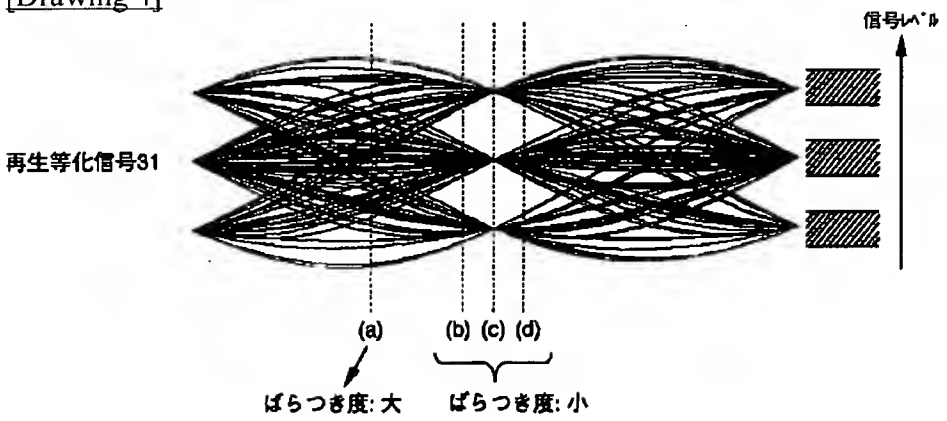
[Drawing 2]



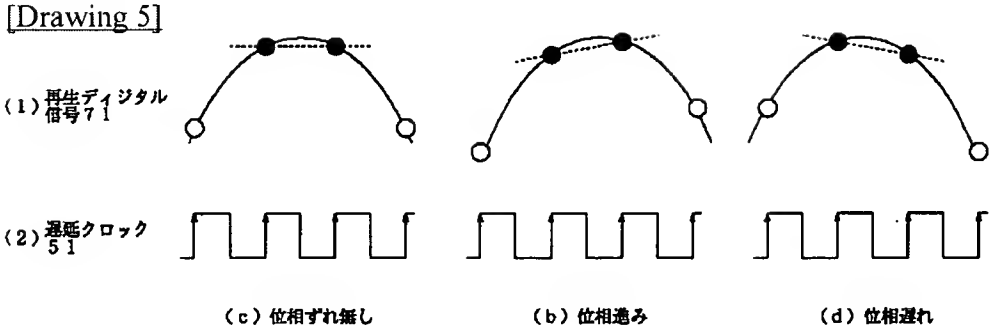
[Drawing 3]



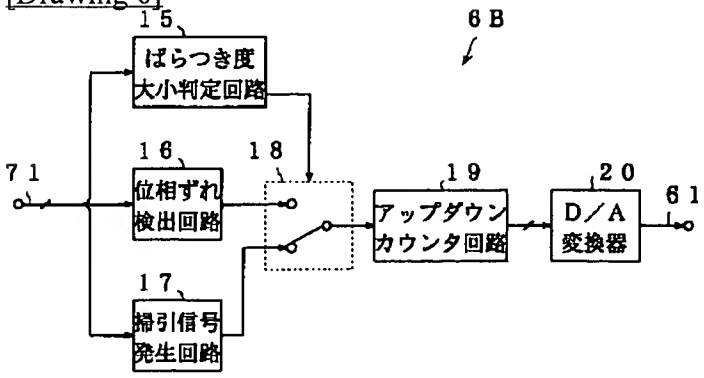
[Drawing 4]



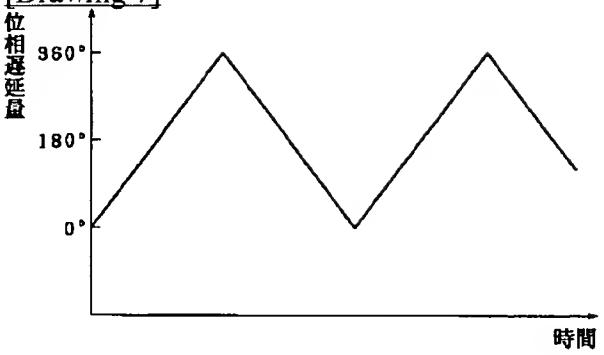
[Drawing 5]



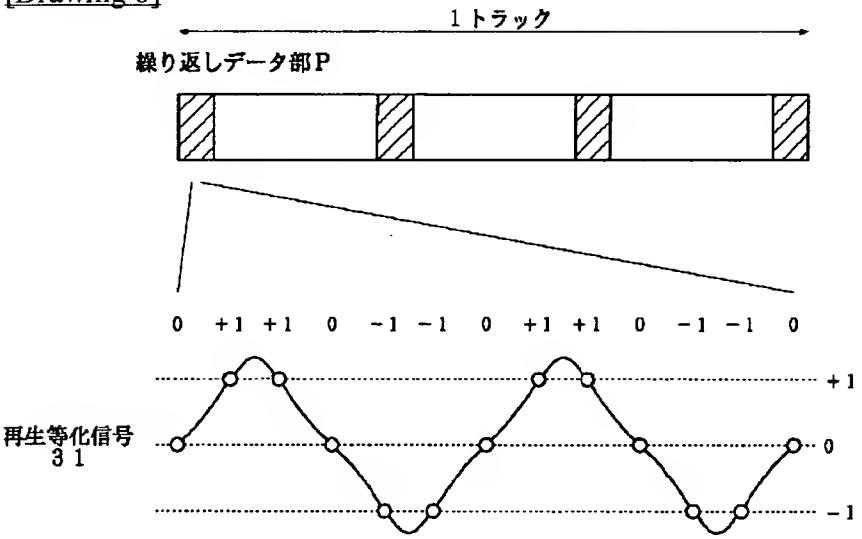
[Drawing 6]



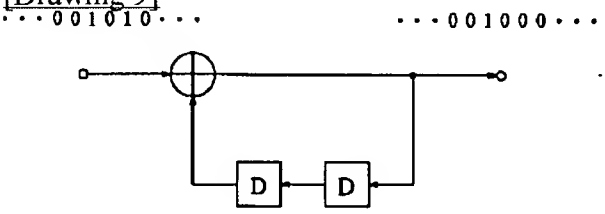
[Drawing 7]



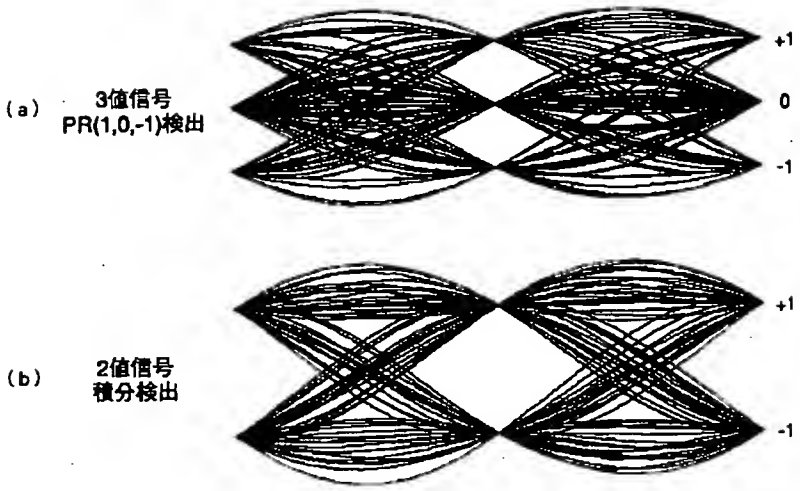
[Drawing 8]



[Drawing 9]



[Drawing 10]



[Translation done.]